WVL

HARRIS SEMICONDUCTOR
A DIVISION OF HARRIS CORPORATION

*Interim device - See ordering information on back page

Preliminary (HX-3210)*

HC-55516/55532

All-Digital Continuously Variable Slope Delta Modulator (CVSD)

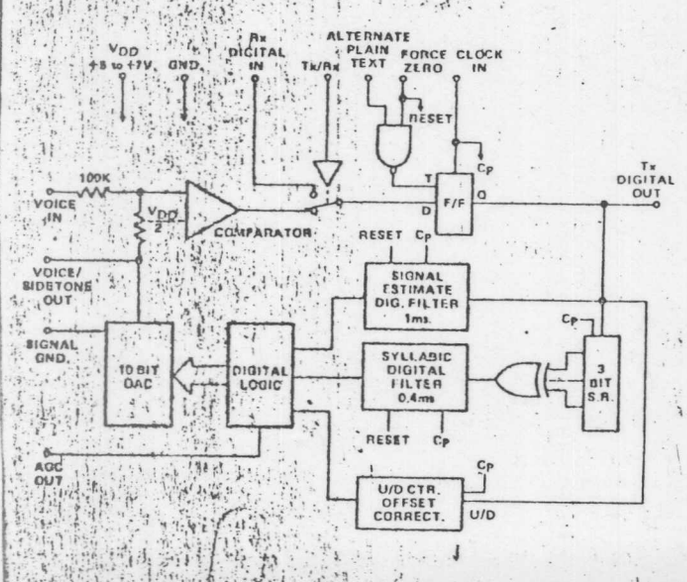
DESCRIPTION

The monolithic circuit covered by this preliminary data sheet is a step size adaptive delta modulator which uses syllabic companding and a single time constant integrator. The necessary logic and digital filters are implemented in high-performance, high-density CMOS logic. Accurate resistor ladders are used to perform the required digital-to-analog conversions.

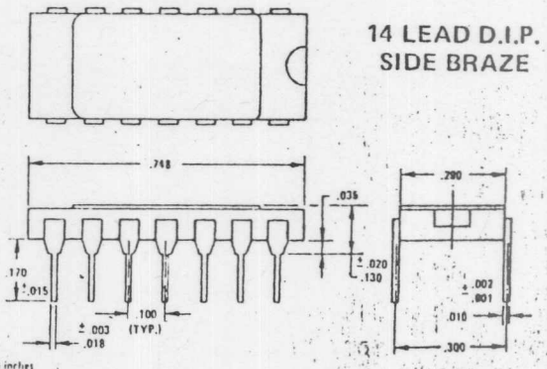
The circuit is able to perform both the encoding and the decoding function, selectable by means of a logic input. To prevent overflow of the digital filters, all computation is inhibited when the input signal exceeds the threshold level. As the input voltage falls below this level, the recovered signal smoothly unclamps. A "quieting" feature is provided to suppress noise in the recovered audio when the input signal energy falls to a low value. During quieting the transmitted digital signal is an alternate 1-0 pattern at one-half the bit rate; the recovered audio has a similar pattern and a peak-to-peak value equal to the minimum step size. Quieting can also be effected by logic inputs to the circuit. A logcial "0" applied to the "alternate plain text" input will cause the quieting pattern to be transmitted without affecting the internal operation of the delta modulator. A logical "0" applied to the "force zero" input will force both the transmitted output and the internal logic into the quieting condition. Means are provided to activate external automatic gain control circuitry if necessary; a logical "0" appears on the "AGC" output when the magnitude of the recovered audio exceeds one-half full scale.

It is recommended that for best voice quality the audio input be band-limited by a low-pass filter to prevent aliasing, and that the recovered voice signal be passed through a low-pass filter to remove out-of-band noise. The characteristics of suitable filters are given in Table II and a schematic of suggested active filters is attached.

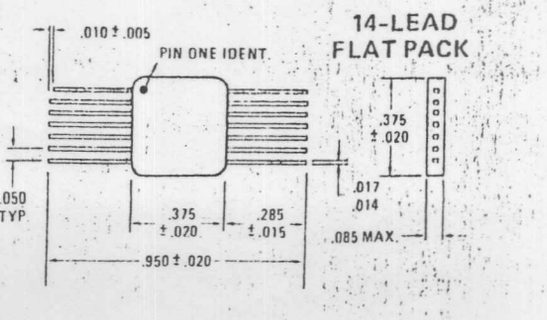
BLOCK DIAGRAM



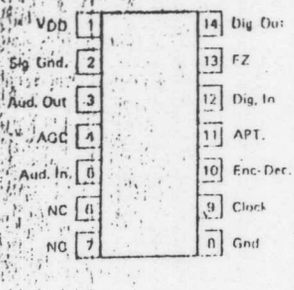
PACKAGES



1. All dimensions in inches
2. All dimensions ±.010 unless otherwise shown

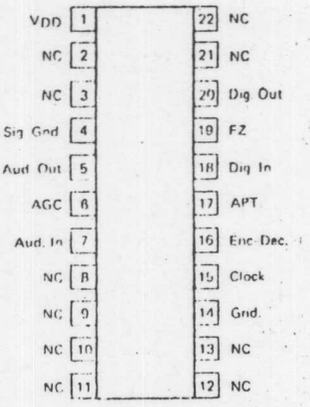


PINOUT PIN ASSIGNMENTS



14 PIN D.I.P. AND FLAT PACK

22 PIN D.I.P. (HX-3210 INTERIM MODEL ONLY)



PIN# 14-LEAD F.P. & D.I.P.	PIN # 22-LEAD D. I. P.	SYMBOL	ACTIVE* LEVEL	DESCRIPTION
1	1	[illegible]		Supply voltage positive.
2	4	[illegible]nd.		Ground connection to D/A ladders and comparator; i. e. [illegible] ground.
3	5	[illegible]ut		Recovered audio out. May be used as side tone at the transmitter. Presents approximately 100 kilohm source. Zero signal reference is $V_{DD}/2$.
4	6	[illegible]		A logic "Low" level will appear at this output when the recovered signal excursion reaches one-half of full scale value.
5	7	[illegible]n		Audio input. Should be externally AC coupled. Presents approximately 100 kilohms in series with $V_{DD}/2$.
8	14	[illegible]		Logic ground. Supply voltage negative.
9	15	Clock		Receiver clock must be phased with digital input such that a positive clock transition occurs near the middle of each received data bit.
10	16	Encode (Decode)	Low	A single CVSD can provide half-duplex operation. The encode and decode functions are selected by the logic level applied to this input. A low level selects the encode mode, a high level, the decode mode.
11	17	APT	Low	Activating this input causes an "alternate plain text" (quieting pattern) to be transmitted without affecting the internal operation of the CVSD.
12	18	Dig. In		Input for the received digital data.
13	19	FZ	Low	Activating this input forces the transmitted output, the internal logic, and the recovered audio output into the "quieting" condition.
14	20	Dig. Out		Output for transmitted digital data.
6	2, 3 8, 13, 21, 22			No internal connection is made to these pins.

*Note: No active input should be left in a "floating" condition.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage At Any Pin	-0.3V to V_{DD} +0.3V
Maximum - V_{DD} Voltage	7.0V
Operating V_{DD} Range	5.0V to 7.0V
Operating Temperature (-9)	-40°C to +85°C
(-2)	-55°C to +125°C
(-8)	-55°C to +125°C
Storage Temperature	-65°C to +150°C

ELECTRICAL CHARACTERISTICS @T_A = 25°C

Test Conditions: V_{DD} = 6.0V, Bit Rate = 16 Kb/s, (HC-55516)
Bit Rate = 32Kb/s (HC-55532)

SUMMARY

Parameter	MIN.	TYP.	MAX.	UNIT	NOTE
Clock Rate	0		64	Kb/s	(1)
Clock Duty	30		70	%	
Supply Voltage	5.0		7.0	V	
Supply Current		1.0		mA	
Digital "1" Input		4.5		V	(2)
Digital "0" Input		1.5		V	(2)
Digital "1" Output		5.5		V	(3)
Digital "0" Output		0.5		V	(3)
Audio Input Voltage		0.5	1.4	Vrms	(4)
Audio Output Voltage		0.5	1.4	Vrms	(5)
Audio Input Impedence		100		KΩ	(6)
Audio Output Impedence		100		KΩ	(7)
Transfer Gain	-0.5		+0.5	db	(8)
Syllabic Time Constant		4.0		mS	(9)
L. P. Filter Time Cosntant		0.94		mS	(9)
Step Size Ratio		24		db	(10)
Resolution		0.1		%	(11)
Min. Step Size		0.2		%	(12)
Slope Overload		Fig. 1			(13)
Signal/Noise Ratio			Tab. 1		(14)
Quieting Audio Out		12		mV	(15)
AGC Threshold		0.5		F. S.	(16)
Clamping Threshold		0.75		F. S.	(17)

NOTES

1. There is one NRZ data bit per clock period. Clock must be phased with digital data such that a positive clock transition occurs in the middle of each received data bit; i. e., the transmitter and receiver clock are in phase.

2. Logic inputs are CMOS compatible at supply voltage and are diode protected. Digital data input is NRZ at clock rate.

3. Logic outputs are CMOS compatible at supply voltage and withstand short-circuits to V_{DD} or ground. Digital data output is NRZ and changes with negative clock transitions.

4. Recommended voice input range for best voice performance.

5. May be used for side-tone in encode mode.

6. Should be externally AC coupled. Presents 100 Kilohms in series with $V_{DD}/2$.

7. Presents 100 Kilohms in series with recovered audio voltage. Zero-signal references is $V_{DD}/2$.

8. Unloaded, for linear signals.

9. At 16 Kb/s. Note that filter time constants are inversely proportional to clock rate.

10. Step size compression ratio of the syllabic filter is defined as the ratio of the filter output, with an equal 1-0 bit density input to the filter, to its minimim output.

11. Minimum quantization voltage level expressed as a percentage of supply voltage.

12. The minimum step size between levels is twice the resolution.

13. At sufficiently high signal amplitude or frequency, the encoder will become slope-overloaded. Figure 1 shows the frequency response at various signal levels, measured with a 3 KHz low-pass filter having a 130 db/octave roll-off to -50 db.

14. Table 1 shows the SNR under various conditions, using the output filter described in 13 (above) at a bit rate of 16 Kb/s. See Table II.

15. The "quieting" or idle-channel audio output is alternate 12 mV steps at one-half the clock rate. The transmitted digital signal is a 1-0 pattern at one-half the bit rate changing on negative clock transitions.

16. A logic "0" will appear at the AGC output pin when the recovered signal reaches one-half or full-scale value; either positive or negative.

17. The recovered signal will be clamped, and the computation will be inhibited, when the recovered signal excursion reaches three-quarters of full-scale value, and will unclamp when it falls below this value.

TABLE I

INPUT FREQUENCY Hz	INPUT AMPLITUDE mV RMS	OUTPUT SNR db MIN.
300	1400	20
300	45	15
1000	500	14
1000	16	9

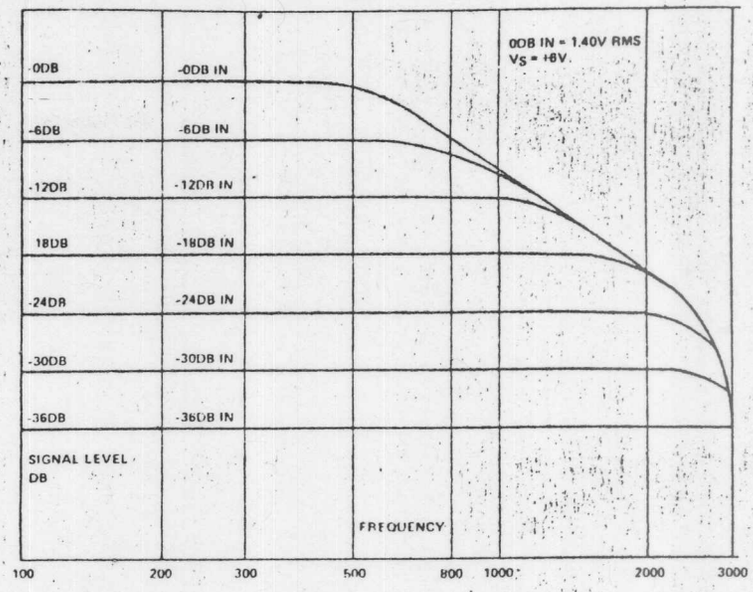


Figure 1 – Transfer Function for CVSD at 16KB

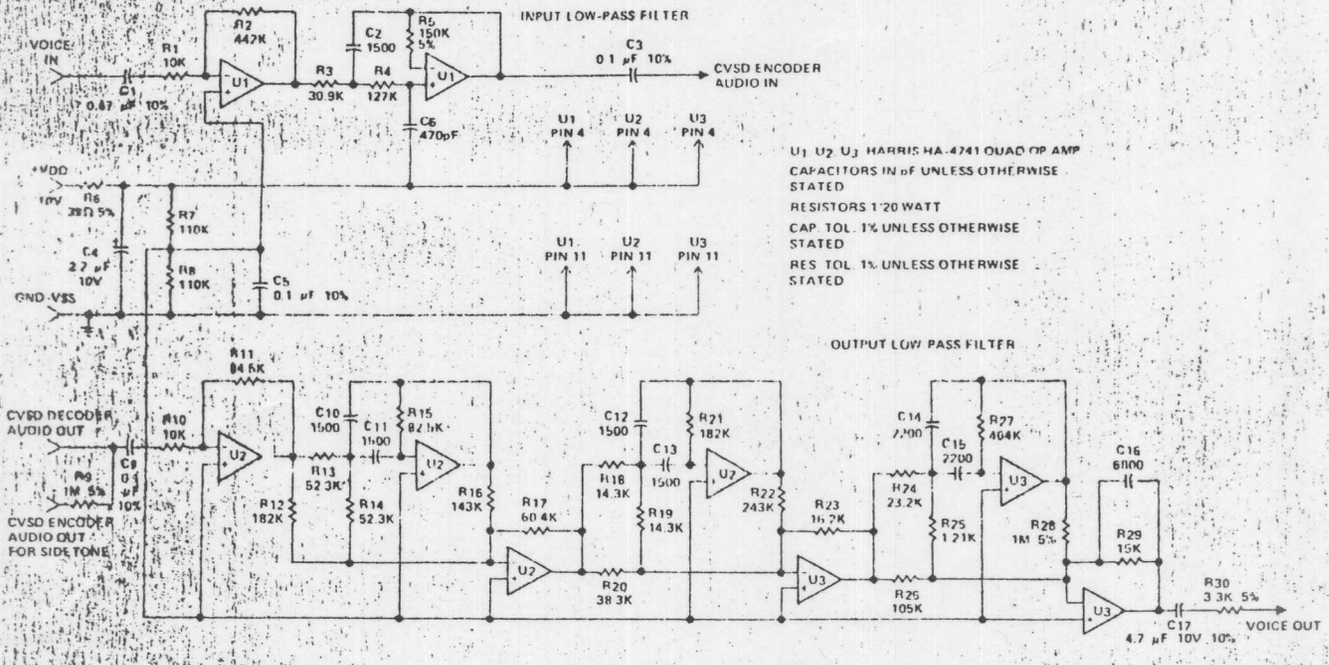


Figure 2 – Suggested Input/Output Audio Filters

TABLE II

INPUT FILTER FREQUENCY RESPONSE		OUTPUT FILTER FREQUENCY RESPONSE	
FREQUENCY	RELATIVE OUTPUT	FREQUENCY	RELATIVE OUTPUT
100 Hz	0±0.5 db	100 Hz to 1500 Hz	0 ± 1.5 db
200 Hz	0±0.1 db	1500 Hz to 3000 Hz	0 ± 2.5 db
1000 Hz	0±0.1 db	3800 Hz to 100 KHz	Less Than –45 db
3000 Hz	-3±0.5 db		
9000 Hz	-20±2 db		